

100V N-Channel Enhancement Mode MOSFET

Description

The XXW100N10D uses advanced **SGTII** technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



TO252-2L

General Features

$V_{DS} = 100V$ $I_D = 100A$

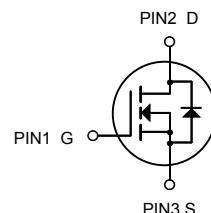
$R_{DS(ON)} < 8.0m\Omega$ @ $V_{GS}=10V$ (**Type: 6.0mΩ**)

Application

Isolated DC

Motor control

Synchronous-rectification



N-Channel MOSFET

Absolute Maximum Ratings ($T_c=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Units
VDS	Drain-Source Voltage	100	V
VGS	Gate-Source Voltage	± 20	V
$I_D@T_A=25^{\circ}\text{C}$	Continuous Drain Current ¹	100	A
$I_D@T_A=70^{\circ}\text{C}$	Continuous Drain Current ¹	68	A
IDM	Pulsed Drain Current ²	210	A
EAS	Single Pulse Avalanche Energy ³	100	mJ
IAS	Avalanche Current	40	A
$P_D@T_A=25^{\circ}\text{C}$	Total Power Dissipation ⁴	100	W
TSTG	Storage Temperature Range	-55 to 150	$^{\circ}\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^{\circ}\text{C}$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	62	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	1.25	$^{\circ}\text{C}/\text{W}$

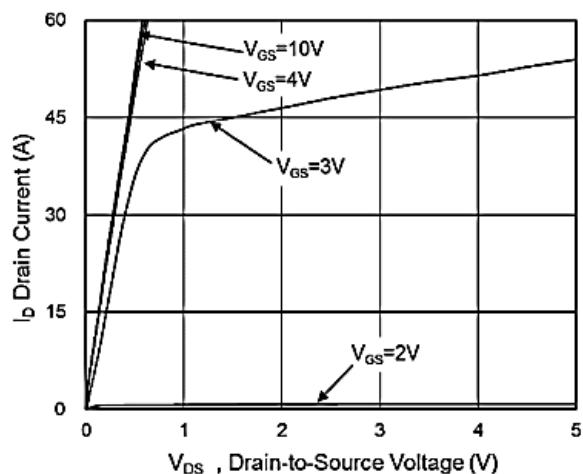
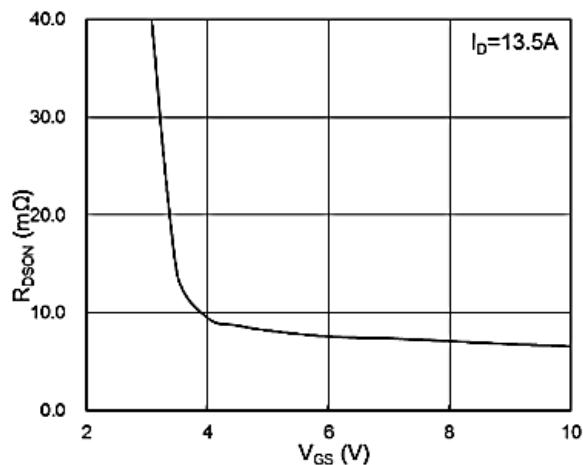
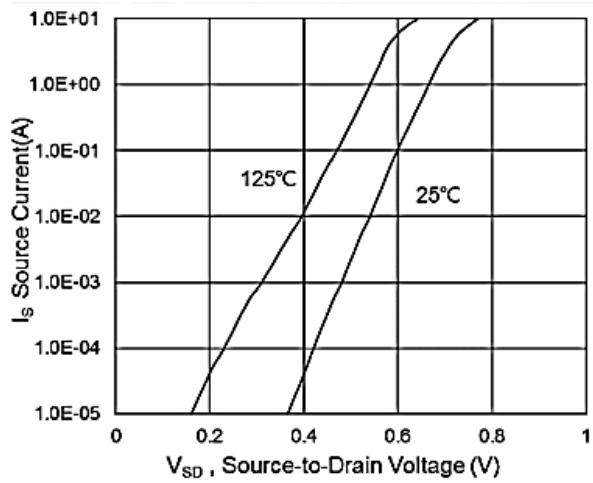
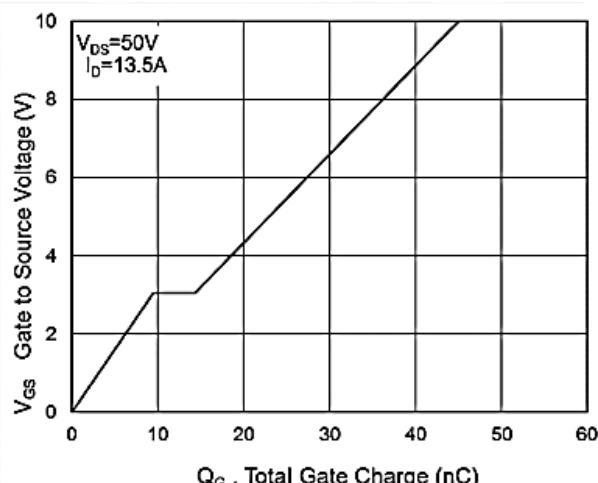
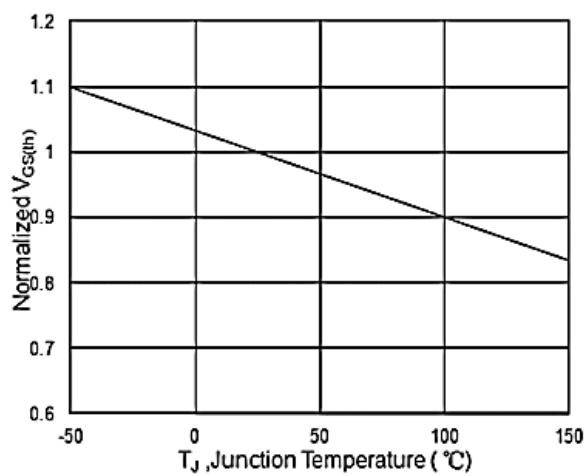
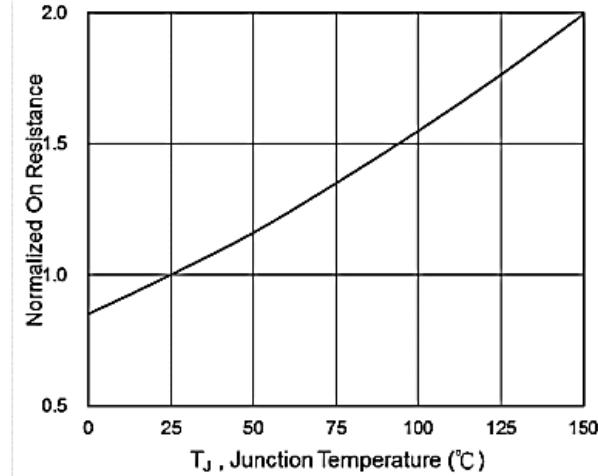
100V N-Channel Enhancement Mode MOSFET

 Electrical Characteristics ($T_c=25^\circ\text{C}$ unless otherwise noted)

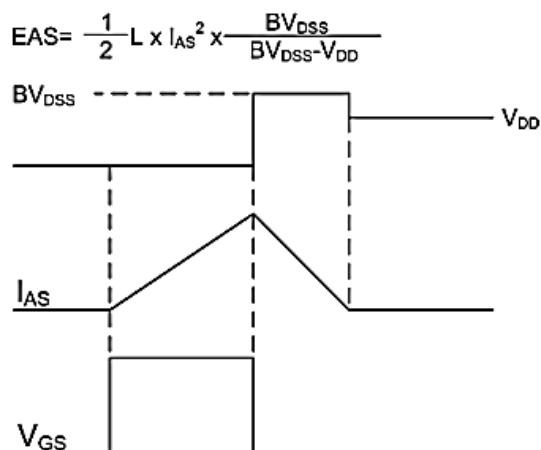
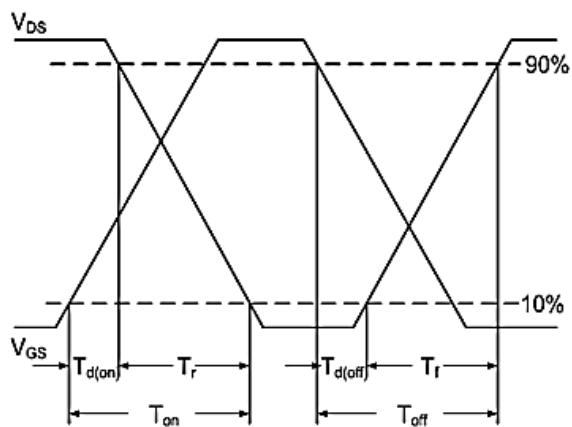
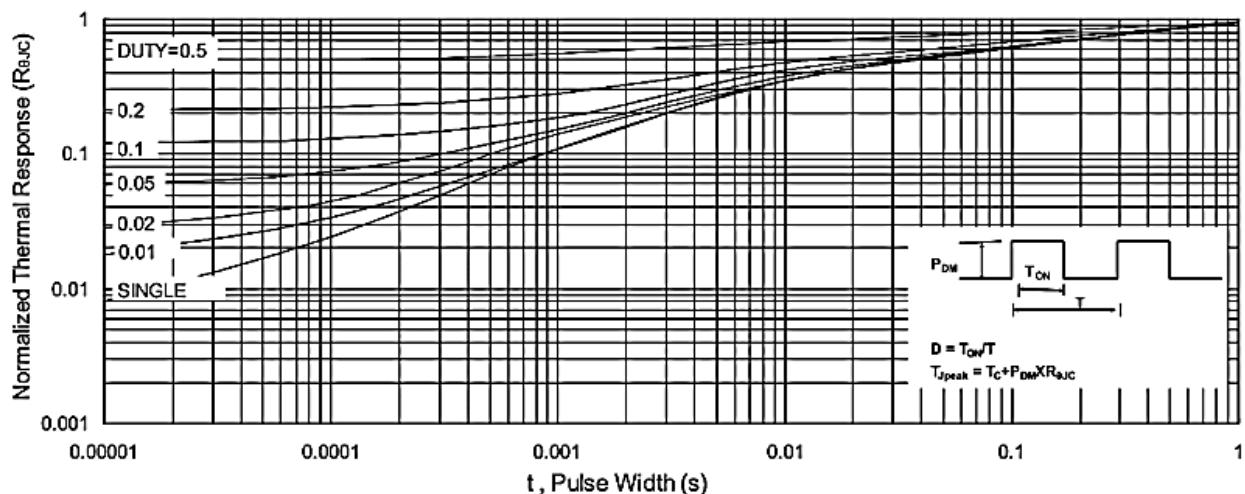
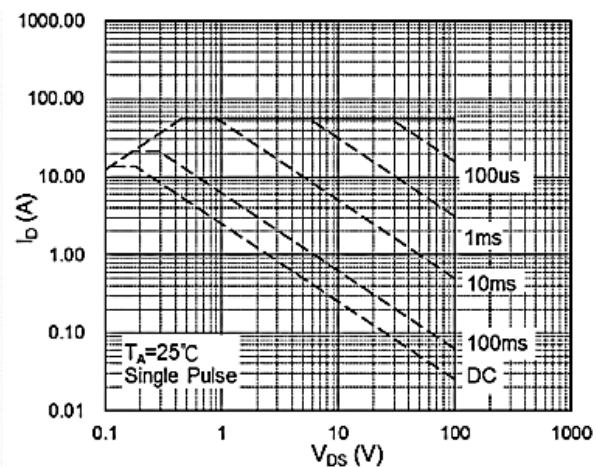
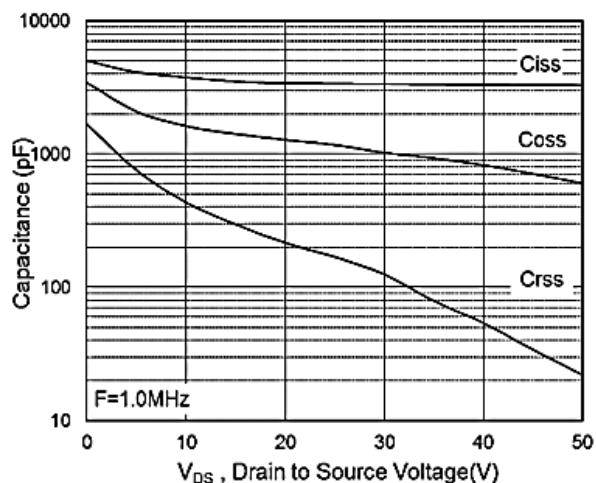
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	100	108	---	V
RDS(ON)	Static Drain-Source On-Resistance ²	$V_{GS}=10\text{V}$, $I_D=13.5\text{A}$	---	6.0	8.0	$\text{m}\Omega$
	Static Drain-Source On-Resistance ²	$V_{GS}=4.5\text{V}$, $I_D=11.5\text{A}$	---	8.7	10.5	
VGS(th)	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=250\mu\text{A}$	1.2	1.8	2.3	V
IDSS	Drain-Source Leakage Current	$V_{DS}=80\text{V}$, $V_{GS}=0\text{V}$, $T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=80\text{V}$, $V_{GS}=0\text{V}$, $T_J=55^\circ\text{C}$	---	---	5	
IGSS	Gate-Source Leakage Current	$V_{GS}=\pm 20\text{V}$, $V_{DS}=0\text{V}$	---	---	± 100	nA
gfs	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=13.5\text{A}$	---	75	---	S
Qg	Total Gate Charge (10V)	$V_{DS}=50\text{V}$, $V_{GS}=10\text{V}$, $ID=13.5\text{A}$	---	45	---	nC
Qg	Total Gate Charge (4.5V)		---	19.3	---	
Qgs	Gate-Source Charge		---	9.5	---	
Qgd	Gate-Drain Charge		---	4.8	---	
Td(on)	Turn-On Delay Time	$V_{DD}=50\text{V}$, $V_{GS}=10\text{V}$, $RG=3\Omega$, $ID=13.5\text{A}$	---	10	---	ns
Tr	Rise Time		---	6.5	---	
Td(off)	Turn-Off Delay Time		---	45	---	
Tf	Fall Time		---	7.5	---	
Ciss	Input Capacitance	$V_{DS}=50\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$	---	3320	---	pF
Coss	Output Capacitance		---	605	---	
Crss	Reverse Transfer Capacitance		---	20	---	
IS	Continuous Source Current ^{1,5}	$V_G=V_D=0\text{V}$, Force Current	---	---	5	A
VSD	Diode Forward Voltage ²	$V_{GS}=0\text{V}$, $I_S=1\text{A}$, $T_J=25^\circ\text{C}$	---	---	1.1	V
trr	Reverse Recovery Time	$IF=13.5\text{A}$, $di/dt=100\text{A}/\mu\text{s}$, $T_J=25^\circ\text{C}$	---	33	---	nS
Qrr	Reverse Recovery Charge		---	150	---	nC

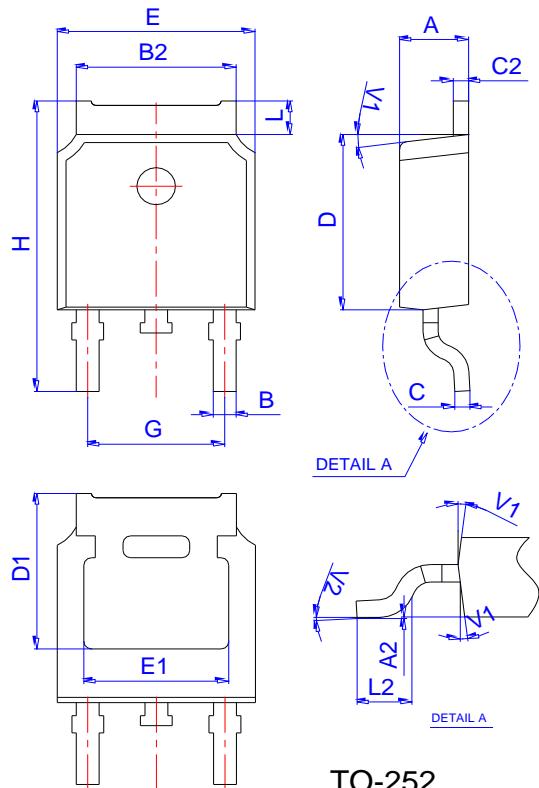
Note :

- 1、The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.
- 2、The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- 3、The EAS data shows Max. rating . The test condition is $V_{DD}=72\text{V}$, $V_{GS}=10\text{V}$, $L=0.1\text{mH}$ $I_{AS}=40\text{A}$
- 4、The power dissipation is limited by 150°C junction temperature
- 5、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation

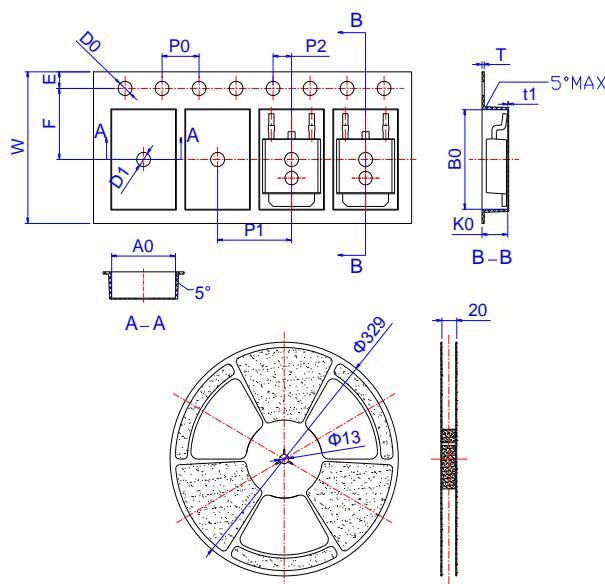
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Typical Characteristics

Fig.1 Typical Output Characteristics

Fig.2 On-Resistance vs. G-S Voltage

Fig.3 Source-Drain Forward Characteristics

Fig.4 Gate-Charge Characteristics

Fig.5 Normalized $V_{GS(th)}$ vs. T_J

Fig.6 Normalized $R_{DS(on)}$ vs. T_J

100V N-Channel Enhancement Mode MOSFET



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Package Mechanical Data:TO-252-3L

TO-252

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Reel Specification-TO-252


Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583